REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-4 and 11-28 are pending in this application. Claims 1, 3, 11, and 13 are amended and Claims 23-28 are added by the present amendment.

Amendments to the claims and new claims find support in the specification as originally filed, at least at page 12, lines 7-24, page 15, lines 9-19, and FIGs. 2-8. Thus, no new matter is added.

In the outstanding Office Action, Claims 1-4 and 11-22 were rejected under 35 U.S.C. §103(a) as unpatentable over U.S. Patent 5,117,380 to Tanagawa in view of U.S. Patent 6,698,662 to Feyt et al. (herein "Feyt").

Initially, Applicant and Applicant's representative gratefully acknowledge the courtesy of a personal interview with Examiner Hoffman on December 10, 2008. During the interview, differences between the claims and the disclosure of the references in the Office Action were discussed. Examiner Hoffman agreed that amended and pending claims discussed during the interview were patentably distinct from the disclosures of the cited references. Comments and claims discussed during the interview are reiterated below.

Amended Claim 1 is directed to a data processing apparatus that includes, in part, an operation processing unit and a pseudo-data generating circuit, which is connected to the data bus, the read control signal output from the operation processing unit, and the write control signal output from the operation processing unit. The pseudo-data generating circuit is configured, in part, to generate pseudo-data and output the generated pseudo-data to the data bus according to an output timing based on the read control signal and the write control signal output from the operation processing unit. The output timing is controlled to cause the pseudo-data generating circuit to output the generated pseudo-data between read or write

cycles and to prevent the pseudo-data generating circuit from outputting the generated pseudo-data during read or write cycles. Independent Claim 11 includes similar features directed to a memory card.

As discussed during the interview, Tanagawa and Feyt fail to teach or suggest each of the features of independent Claims 1 and 11. For example, Tanagawa and Feyt fail to teach or suggest output timing that is controlled to cause a pseudo-data generating circuit to output the generated pseudo-data between a read cycle and an immediately following write cycle, and prevent the pseudo-data generating circuit from outputting the generated pseudo-data during the read cycle and the immediately following write cycle.

Tanagawa describes a random number generator that is driven by clock pulses from a clock source independent of a system clock source.[1] According to Tanagawa, a random number generator generates random numbers based on clock signals that operate independent of a system clock, and the random numbers are output to the data base based on a timing of only a read signal RD.[2]

Feyt describes initiating a programming of an EEPROM followed by effecting cryptographic calculation.[3] Further, Feyt describes a process that includes "2-presentation, on the data bus, of the data item to be written, ... 4-initiation of the programming, 5-waiting during the programming time, 6-stopping the programming."[4]

However, as discussed during the interview, Tanagawa and Feyt are silent regarding any outputting of random numbers based on a timing of a write signal from an operation processing unit, and Tanagawa and Feyt are silent regarding output timing that is controlled to cause a circuit to output generated pseudo-data between read or write cycles and to prevent the circuit from outputting the generated pseudo-data during read or write cycles.

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[1] Tanagawa at Abstract.
[2] Tanagawa at column 3, lines 8-18.
[3] Feyt at column 3, lines 39-50.
[4] Feyt at column 3, lines 20-25.

Therefore, as discussed during the interview, Claims 1 and 11, and claims depending therefrom, patentably define over Tanagawa and Feyt.

Claim 3 is directed to a data processing apparatus that includes, in part, an operation processing unit, a data bus connected to the operation processing unit, a memory and a control signal generating circuit. The control signal generating circuit is configured to receive a read signal and a write signal from the operation processing unit, detect a change in the read signal and a change in the write signal, and generate a control signal based on the detected change. The pseudo-data generating circuit is connected to the data bus and configured to receive the control signal from the control signal generating circuit, generate pseudo-data, and output the generated pseudo-data to the data bus in accordance with a timing of the control signal. Independent Claim 13 includes similar features.

As discussed during the interview, Tanagawa and Feyt also fail to teach or suggest each of the features of Claim 3 or 13. For example, as discussed during the interview, Tanagawa and Feyt fail to teach or suggest generating pseudo-data and outputting the generated pseudo-data to a data bus in accordance with a timing of a control signal that is based on a detected change in a read signal and a write signal.

Therefore, as discussed during the interview, Claims 1 and 11, and claims depending therefrom, also patentably define over Tanagawa and Feyt.

As discussed during the interview, Tanagawa and Feyt also fail to teach or suggest controlling the output timing of the generated pseudo-data to be delayed by a predetermined time from at least one of the active read control time period and the active write control time period, as recited in Claims 16, 18, 20, and 22. Therefore, Claims 16, 18, 20, and 22 patentably define over Tanagawa and Feyt for that

independent reason in addition to the reasons noted above with respect to the independent claims.

In addition, as discussed during the interview, Tanagawa and Feyt also fail to teach or suggest that the predetermined time period is shorter than the active read control time period or the active write control time period, as recited in Claims 23-26. Therefore, Claims 23-26 patentably define over Tanagawa and Feyt for that independent reason in addition to the reasons noted above with respect to the independent claims.

New Claim 27 is directed to a data processing apparatus that includes an operation processing unit and a dummy circuit. The dummy circuit is configured to consume power and not consume power according to an output timing based on a read control signal and a write control signal output from the operation processing unit. As discussed during the interview, Tanagawa and Feyt also fail to teach or suggest those features.

New Claim 28 is directed to a data processing apparatus that includes a dummy circuit connected to a data bus and configured to receive a control signal from a control signal generating circuit, consume power, and not consume power in accordance with a timing of the control signal. As discussed during the interview, Tanagawa and Feyt also fail to teach or suggest those features.

Accordingly, it is respectfully submitted that independent Claims 1, 3, 11, 13, 27, and 28, and claims depending therefrom, are allowable.

Consequently, in light of the above discussion and in view of the present amendment this application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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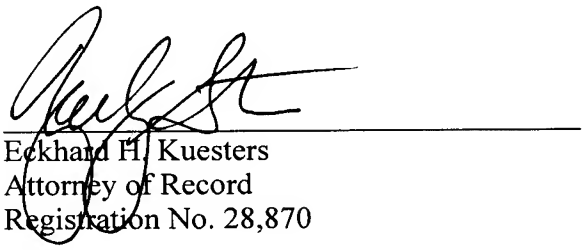

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